

A Report on
End-to-End SoC Verification Architecture, DV & PD
Roles with UVM Testbench and Coverage Closure

Aim: Academic focuses on basic digital logic and standard Verilog/VHDL, industrial chip design requires massive automation frameworks, complex protocols, and strict sign-off constraints build to bridge the gap between academic theory and industry reality of the competencies, mindset, and strategies needed to excel.



The poster is for a guest lecture organized by the Department of Electronics & Communication Engineering. It features a photo of the speaker, Ajay Kumar, a Functional Verification Engineer from VALSOC Semiconductor Industry. The title of the lecture is "End-to-End SoC Verification: Architecture, DV & PD Roles with UVM Testbench and Coverage Closure". The event is scheduled for 11th September 2026 at 10:00 AM in the ECE Seminar Hall, II Floor. The poster includes logos for Nalla Narasimha Reddy Group of Institutions, NNRG, NAAC, NBA, and IETE.

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Department of Electronics & Communication Engineering

Organize
Guest Lecture
on
End-to-End SoC Verification:
Architecture, DV & PD Roles with UVM
Testbench and Coverage Closure

Ajay Kumar
Functional Verification Engineer
VALSOC Semiconductor Industry

Date: 11th September 2026 **Venue: ECE Seminar Hall, II Floor** **Time: 10:00 AM**

The Department of ECE, organized a Guest Lecture on “**End-to-End SoC Verification Architecture, DV & PD Roles with UVM Testbench and Coverage Closure**” on 11th September 2026 in association with VALSOC Semiconductor Industry. The session commenced at 10:00 A.M. and the student participants are 200 Members.

The programme commenced with a warm welcome address delivered by the Dr. Hari Prasad Professor of ECE. The Dr. Hari Prasad extended a cordial welcome to the Chief Guest, faculty members and students emphasizing the significance of the theme “**End-to-End SoC Verification Architecture, DV & PD Roles with UVM Testbench and Coverage Closure**”. The address highlighted the importance The session provided a comprehensive overview of SoC verification architectures, the distinct roles of Design Verification (DV) and Physical Design (PD) engineers, UVM testbench methodologies, and the critical importance of achieving coverage closure before chip fabrication in today's competitive world. The Dr. Hari Prasad encouraged the participants to actively engage in the session and make the best use of the valuable insights shared by the resource person.



End-to-End SoC Verification Architecture

Mr. Ajay Kumar introduced the complexities of modern SoC architectures, which integrate multiple IP cores, processors, memory subsystems, and high-speed interfaces. Transitioning from block-level verification to subsystem and full-chip SoC verification. Ensuring robust data routing across complex Network-on-Chip (NoC) and Advanced Microcontroller Bus Architecture (AMBA) protocols like AXI, AHB, and APB. Addressing challenges introduced by multi-voltage domains and power management infrastructures.

Career & Professional Development

Students can now clearly distinguish between Design Verification (DV) and Physical Design (PD) career tracks, helping them align their elective courses and skill development. The session bridged the gap between academic VLSI design curriculum's and the fast-paced requirements of modern semiconductor companies like VALSOC.

The event is witnessed by the Dr Hariprassd Professor of ECE as well as concerned Faculty coordinator of the event Mr. K Srinivas and other faculties V.V Nandini , K Ramesh



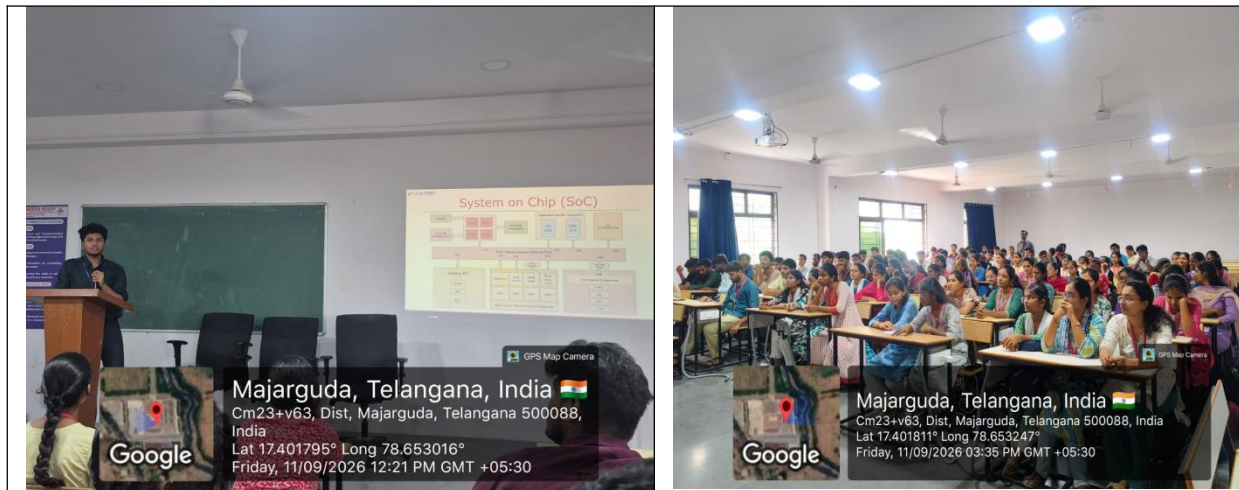
Speaker Mr. Ajay Kumar enlightening the career opportunities to the participants



Speaker Mr. Ajay Kumar from addressing the students in the program

Feedback has been given by a couple of students and the presentation was evaluated with a score of **8.0 out of 10**, reflecting a favorable overall response and indicating opportunities for further enhancement. Students appreciated the session, commenting that it was good, informative, useful, and provided valuable insights about the career opportunities after graduation

Finally, the vote of thanks by expressing gratitude to the resource persons, faculty members, and students for their enthusiastic participation and contribution towards the successful conduct of the event. The programme concluded at 12:30 PM.



Outcome: The session enhanced participants' understanding of the importance of understood how complex System-on-Chip (SoC) architectures handle data flow and communication protocols like AMBA AXI, and The event provided students and faculty an open channel to connect with an active industry professional, opening doors for potential mentorship or project guidance and the department successfully introduced industry-validated practices into the academic ecosystem in engineering field.

Event Co-Ordinator (Mr. K Srinivas)

**HoD-ECE
(Dr. Ravi Bolimera)**